Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A semiconductor device, comprising a substrate;

an active area formed within the substrate;

a first non-planar metallization level which is formed on the substrate and is in contact with the active area; and

a second planar metallization level arranged spaced apart from the first metallization level above the substrate and connected to the first metallization level via a through connection.

2. (currently amended) The semiconductor device according to claim 1, wherein the semiconductor device includes a field effect transistor having a gate, a source area and a drain area, wherein the first non-planar metallization level includes a first portion connected to the source area, a second portion connected to the drain area and a third portion at least partially covering the gate, and wherein the second planar metallization level includes at least one portion connected to the ~~first portion of the first non-planar metallization level or to the~~ second portion of the first non-planar metallization level.

3. (original) The semiconductor device according to claim 2, wherein the first portion and the third portion of the first non-planar metallization level are connected.

4. (original) The semiconductor device according to claim 2, wherein between the first non-planar metallization level and the second planar metallization level an insulating layer is arranged, wherein in the insulating layer at least one through connection for a connection of the first non-planar metallization level to the second planar metallization level is formed.

5. (original) The semiconductor device according to claim 2, wherein the third portion is implemented to shield the gate against electrostatic or electrodynamic interferences.

6. (currently amended) An amplifier circuit comprising a field effect transistor ~~according to claim 2~~ comprising:

a substrate;

an active area formed within the substrate comprising a gate, a source area and a drain area;

a first non-planar metallization level which is formed on the substrate and is in contact with the active area; and

a second planar metallization level arranged spaced apart from the first metallization level above the substrate and connected to the first metallization level via a through connection; and,

wherein the first non-planar metallization level includes a first portion connected to the source area, a second portion connected to the drain area and a third portion at least partially covering the gate, and wherein the second planar metallization level includes at

least one portion connected to the second portion of the first non-planar metallization level.

7. (new) The amplifier circuit of claim 6, wherein the first portion and the third portion of the first non-planar metallization level are connected.

8. (new) The amplifier circuit of claim 6, wherein between the first non-planar metallization level and the second planar metallization level an insulating layer is arranged, wherein in the insulating layer at least one through connection for a connection of the first non-planar metallization level to the second planar metallization level is formed.

9. (new) The amplifier circuit of claim 6, wherein the third portion is implemented to shield the gate against electrostatic or electrodynamic interferences.

10. (new) The semiconductor device according to claim 1, wherein the semiconductor device includes a field effect transistor having a gate, a source area and a drain area, wherein the first non-planar metallization level includes a first portion connected to the source area, a second portion connected to the drain area and a third portion at least partially covering the gate, and wherein the second planar metallization level includes at least one portion connected to the first portion of the first non-planar metallization level.

11. (new) The semiconductor device according to claim 10, wherein the first portion and the third portion of the first non-planar metallization level are connected.

12. (new) The semiconductor device according to claim 10, wherein between the first non-planar metallization level and the second planar metallization level an insulating

layer is arranged, wherein in the insulating layer at least one through connection for a connection of the first non-planar metallization level to the second planar metallization level is formed.

13. (new) The semiconductor device according to claim 10, wherein the third portion is implemented to shield the gate against electrostatic or electrodynamic interferences.

14. (new) A semiconductor device comprising:

a substrate;

active areas formed within the substrate comprising a source area and a drain area;

a gate disposed between the source area and the drain area and insulated from the substrate by an oxide layer;

a first non-planar metallization level formed on the substrate in contact with the active areas including a first portion connected to the source area, a second portion connected to the drain area and a third portion at least partially covering the gate, the third portion including a portion extending downwardly between the gate and the second portion and terminating at an end displaced from the substrate by a displacement; and

a second planar metallization level arranged spaced apart from the first metallization level above the substrate and connected to the second portion of the first metallization level via a through connection.

15. (new) The semiconductor device of claim 14, wherein the first portion and the third portion of the first non-planar metallization level are connected.

16. (new) The semiconductor device of claim 14, wherein between the first non-planar metallization level and the second planar metallization level an insulating layer is arranged, wherein in the insulating layer at least one through connection for a connection of the first non-planar metallization level to the second planar metallization level is formed.

17. (new) The semiconductor device of claim 15, wherein the third portion is implemented to shield the gate against electrostatic or electrodynamic interferences.

18. (new) The semiconductor device of claim 15, wherein the third portion is spaced apart from the second portion and the displacement is less than about 500 nm.

19. (new) The semiconductor device of claim 18, and further comprising an oxide layer disposed between the third portion and the gate.

20. (new) The semiconductor device of claim 19, and further comprising a reduced surface field area formed in the substrate and disposed between the gate and the drain area.